

### APN6014LT3G

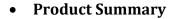
### **60V N-Channel Enhancement Mode MOSFET**

### • General Description

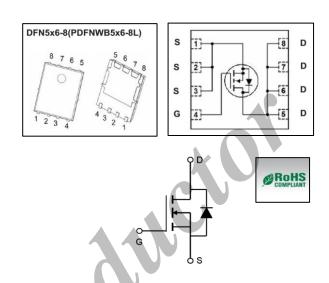
APN6014LT3G combines advanced MOSFET technology with a low resistance package to provide extremely low  $R_{\text{DS(ON)}}.$  This device is most suitable to load-switch or DC/DC conversion applications.

### Applications

- $\,$  DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial



$ m V_{DS}$	60V
ID	95A
$R_{DS(ON)}$ (at $V_{GS} = 10V$ )	$< 2.5 \text{m}\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	< 3.4mΩ



### Absolute Maximum Ratings (Ta = 25<sup>12</sup> unless otherwise specified)

Parameter	Symbol	Rating	Unit		
Drain-Source Voltage	$V_{DS}$	60	V		
Gate-Source Voltage	$V_{GS}$	±20	V		
Continuous Drain Current A Ta = 25°C	$I_D$	95	A		
Ta = 70°C		60			
Pulsed Drain Current B	$I_{DM}$	390			
Single Pulse Avalanche Energy <sup>C</sup>	E <sub>AS</sub>	500	mJ		
Power Dissipation D	$P_D$	120	W		
Junction and Storage Temperature Range	$T_J$ , $T_{STG}$	-55 to 150	°C		
Thermal Characteristics					
Thermal Resistance. Junction-to-Ambient <sup>E</sup>	$R_{\theta JA}$	20	°C/W		
Thermal Resistance. Junction-to-Case	$R_{ heta JC}$	1.04	C/ VV		

#### Notes

A. The maximum current rating is package limited.

B. Repetitive rating; pulse width limited by maximum junction temperature.

C.  $V_{DD}$ =50 V,  $R_G$ =25  $\Omega$ , L=0.5mH, starting  $T_j$ =25°C

D.  $P_D$  is based on maximum junction temperature, using junction-case thermal resistance.

E. The value of Reia is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. copper in a still air environment with Ta=25 ć.



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### • Electrical Characteristics (T<sub>J</sub> = 25<sup>12</sup> unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static Characteristics						2	
Drain-Source Breakdown Voltage	$V_{DSS}$	$I_D = 250 \mu A$ , $V_{GS} = 0 V$	60			V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}$ =60V, $V_{GS}$ =0V			1	μΑ	
Gate-Body Leakage Current	$I_{GSS}$	$V_{DS}$ =0V, $V_{GS}$ =±20V			±100	nA	
On Characteristics							
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	1.2	1.8	2.2	V	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		2.1	2.5	mΩ	
	TCDS(ON)	$V_{GS}$ =4.5V, $I_D$ =15A	A	2.7	3.4	11177	
Dynamic Characteristics							
Input Capacitance	$C_{iss}$		1	5950			
Output Capacitance	$C_{oss}$	$V_{GS}$ =0V, $V_{DS}$ =25V, f=100KHz		1250		pF	
Reverse Transfer Capacitance	$C_{\mathrm{rss}}$			85			
Switching Characteristics							
Total Gate Charge	$Q_{\rm g}$			93			
Gate Source Charge	$Q_{\mathrm{gs}}$	$V_{GS}=10V, V_{DS}=50V, I_{D}=50A$		17		nC	
Gate Drain Charge	$Q_{\mathrm{gd}}$			14			
Turn-On Delay Time	t <sub>D(on)</sub>			22.5			
Turn-On Rise Time	$t_{r}$	$V_{GS}=10V, V_{DD}=30V,$		6.7		na	
Turn-Off Delay Time	$t_{D(off)}$	$I_D=25A R_{GEN}=2\Omega$		80.3		ns	
Turn-Off Fall Time	$t_{\rm f}$			26.9			
Drain-Source Diode Characteristics	Viv						
Body Diode Reverse Recovery Time	$t_{rr}$	I -25A d /d -100A /ua		68		ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$	$I_F$ =25A, $d_i/d_t$ =100A/ $\mu$ s		73		nC	
Diode Forward Voltage	$V_{SD}$	$V_{GS}$ =0V, $I_S$ =20A			1.2	V	

### Ordering Information

Ordering Part Number	Package	MOQ
APN6014LT3G	DFN5x6-8 (PDFNWB5x6-8L)	5,000 pcs / reel

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# APN6014LT3G

## **60V N-Channel Enhancement Mode MOSFET**

### Typical Electrical and Thermal Characteristics

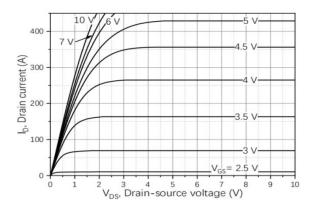


Figure 1. Output Characteristics

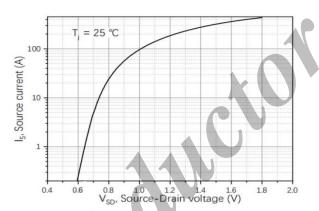


Figure 2. Transfer Characteristics

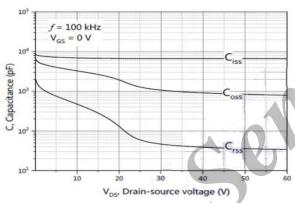


Figure 3. Capacitance Characteristics

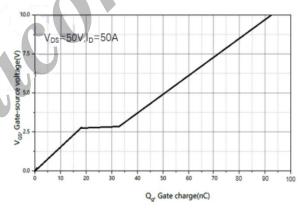


Figure4. Gate Charge

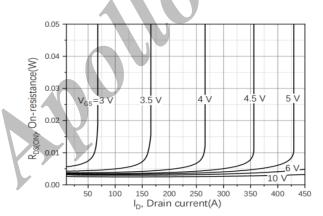


Figure 5. Drain-Source on Resistance

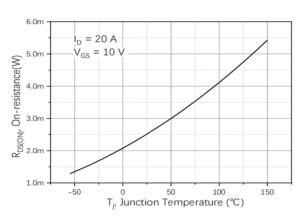


Figure 6. Drain-Source on Resistance

### • Typical Electrical and Thermal Characteristics

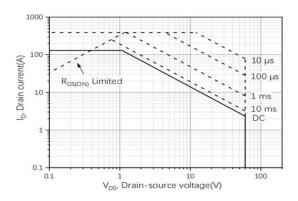


Figure 7. Safe Operation Area

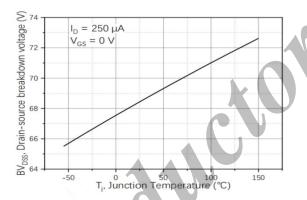


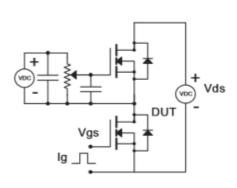
Figure8. Drain-source breakdown voltage

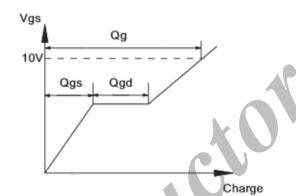


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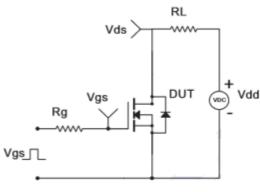
## **60V N-Channel Enhancement Mode MOSFET**

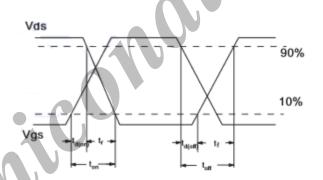
### Gate Charge Test Circuit & Waveform



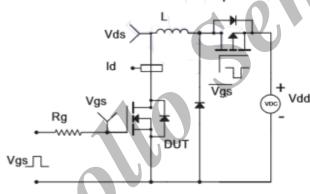


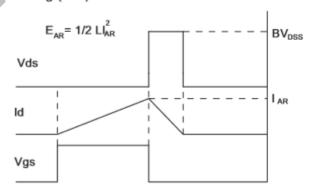
### Resistive Switching Test Circuit & Waveforms



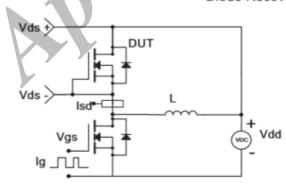


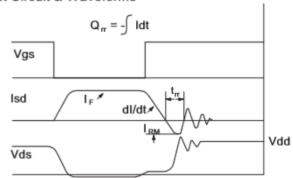
#### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



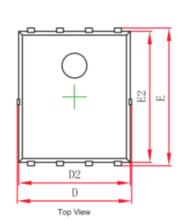


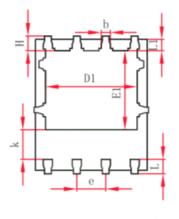
#### Diode Recovery Test Circuit & Waveforms



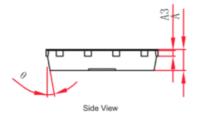


### • DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



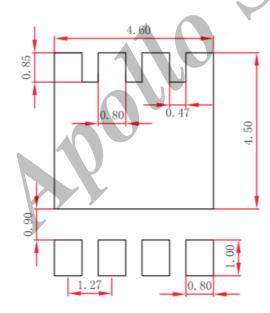


Bottom View



Tiew fiew					
0	Dimensions in Millimeters		Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
A	0,900	1.000	0. 035	0.039	
A3	0.25	REF.	0. 010REF.		
D	4.941	5.096	0. 195	0. 201	
E	5.974	6.126	0. 235	0.241	
D1	3.910	4.110	0.154	0.162	
E1	3, 375	3.575	0.133	0.141	
D2	4,824	4.976	0.190	0.196	
E2	5. 674	5.826	0. 223	0. 229	
k	1.190	1.390	0. 047	0.055	
ь	0.350	0.450	0.014	0.018	
e	1, 27		0.050		
L	0.559	0.711	0.022	0.028	
L1	0.424	0.576	0.017	0.023	
H	0.574	0, 726	0.023	0.029	
9	10*	12*	10*	12*	

### ■ DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



#### Note:

- 1. Controlling dimension:in millimeters.
- 2.General tolerance:±0.05mm.
- 3. The pad layout is for reference purposes only.



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