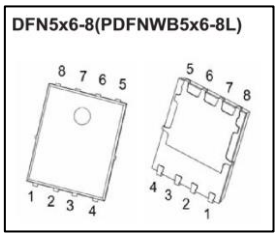
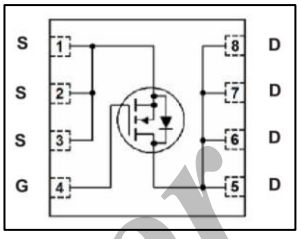
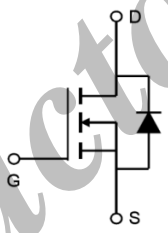
APN6512
30V N-Channel Enhancement Mode MOSFET







RoHS COMPLIANT

Pb Pb-Free

- **General Description**

APN6512 combines advanced MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is most suitable to load-switch or DC/DC conversion applications.

- **Applications**

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

- **Product Summary**

V_{DS}	30V
I_{DMAX} (at V_{GS} = 10V)	150A
$R_{DS(ON)}$ (at V_{GS} = 10V)	< 1.7 mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 2.4 mΩ

- **Absolute Maximum Ratings Ta = 25℃**

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [G]	Tc=25℃	I_D	150	A
	Tc=100℃		115	
Pulsed Drain Current [C]		I_{DM}	340	
Continuous Drain Current	TA=25℃	I_{DSM}	54	
	TA=25℃		43	
Avalanche Current [C]		I_{AS}	70	
Avalanche Energy L = 0.05 mH [C]		E_{AS}	123	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	V
Power Dissipation [B]	Tc=25℃	P_D	83	W
	Tc=100℃		33	
Power Dissipation [A]	TA=25℃	P_{DSM}	7.4	
	TA=70℃		4.7	
Thermal Resistance.Junction- to-Ambient [A]	t ≤ 10s	R_{thJA}	17	℃/W
Thermal Resistance.Junction- to-Ambient [A D]	Steady-State		55	
Thermal Resistance.Junction- to-Case	Steady-State	R_{thJC}	1.5	
Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{stg}	-55 to 150	

Notes:

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

G. The maximum current rating is package limited.

- **Electrical Characteristics (T_J = 25℃ unless otherwise specified)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250 µA, V_{GS} = 0V	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 ℃			5	
Gate to Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250µA	1		2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A			1.7	mΩ
		V_{GS} = 10 V, I_D = 20 A, T_J = 125 ℃			2.3	
		V_{GS} = 4.5 V, I_D = 20 A			2.4	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 20 A		85		S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		3430		pF
Output Capacitance	C_{oss}			1327		
Reverse Transfer Capacitance	C_{rss}			175		
Gate Resistance	R_g	V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	0.3		1.1	Ω
Total Gate Charge	Q_g(10V)	V_{GS} = 10V, V_{DS} = 15 V, I_D = 20 A		53	64	nC
Total Gate Charge	Q_g(4.5V)			25	30	
Gate Source Charge	Q_{gs}			7.8		
Gate Drain Charge	Q_{gd}			10.3		
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 15 V, R_L = 0.75 Ω, R_{GEN} = 3 Ω		7.5		ns
Turn-On Rise Time	t_r			5.0		
Turn-Off DelayTime	$t_{d(off)}$			33.8		
Turn-Off Fall Time	t_f			9.8		
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, dI/dt = 500 A/µs		22		
Body Diode Reverse Recovery Charge	Q_{rr}			58		nC
Maximum Body-Diode Continuous Current	I_S				85	A
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1 A			1	V

Notes:

E. The static characteristics in Figures 1 to 6 are obtained using <300s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

- **Ordering Information**

Ordering Part Number	Package	MOQ
APN6512	DFN5x6-8 (PDFNWB5x6-8L)	5,000 pcs / reel

- **Typical Characteristics**

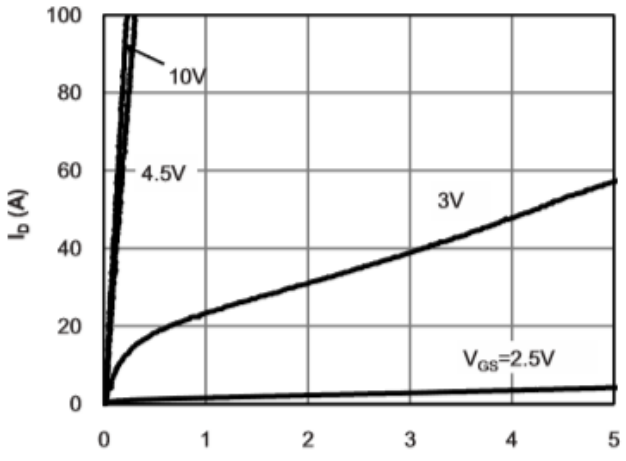


Fig 1: On-Region Characteristics (Note E)

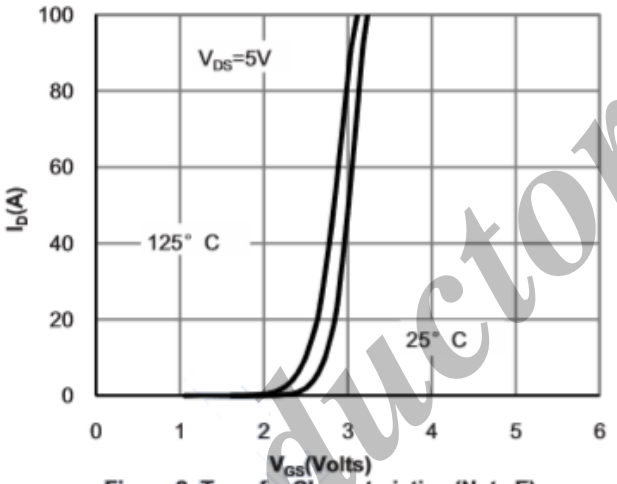


Figure 2: Transfer Characteristics (Note E)

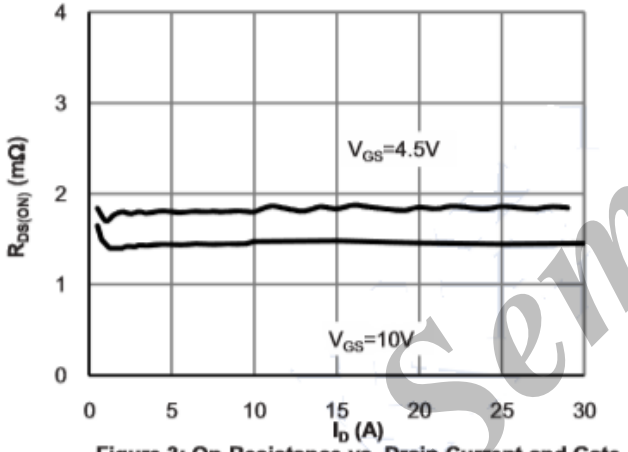


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

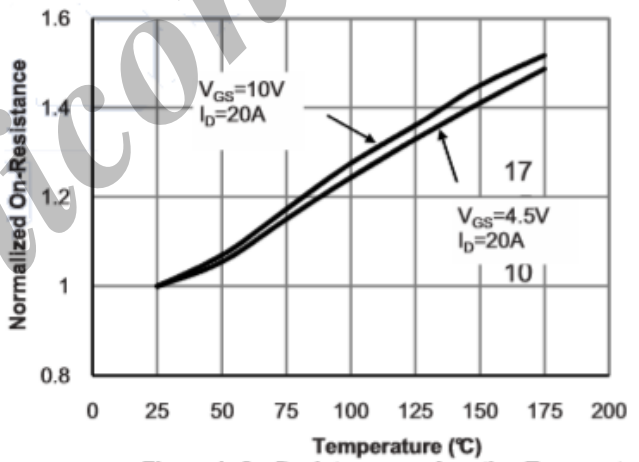


Figure 4: On-Resistance vs. Junction Temperatu (Note E)

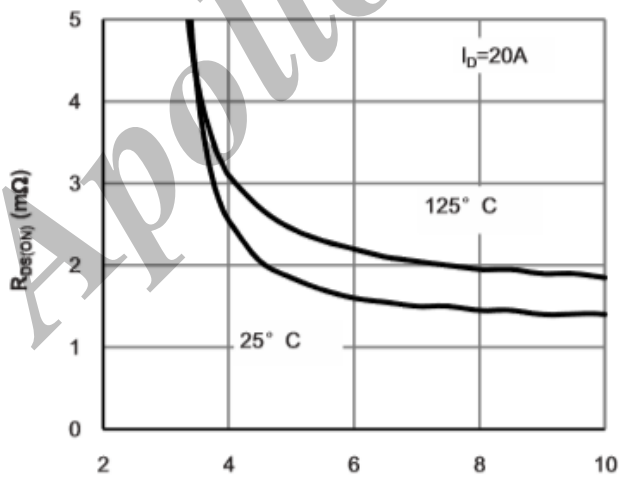


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

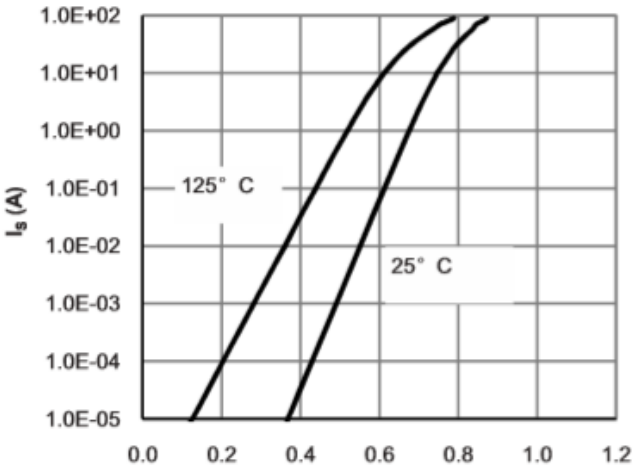


Figure 6: Body-Diode Characteristics (Note E)

- **Typical Characteristics**

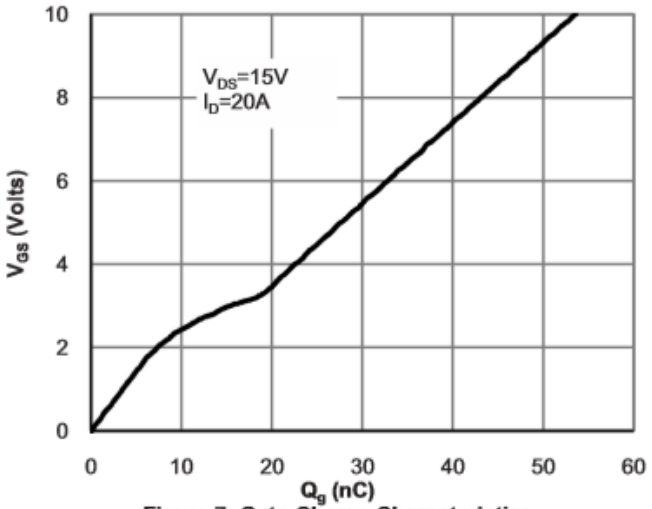


Figure 7: Gate-Charge Characteristics

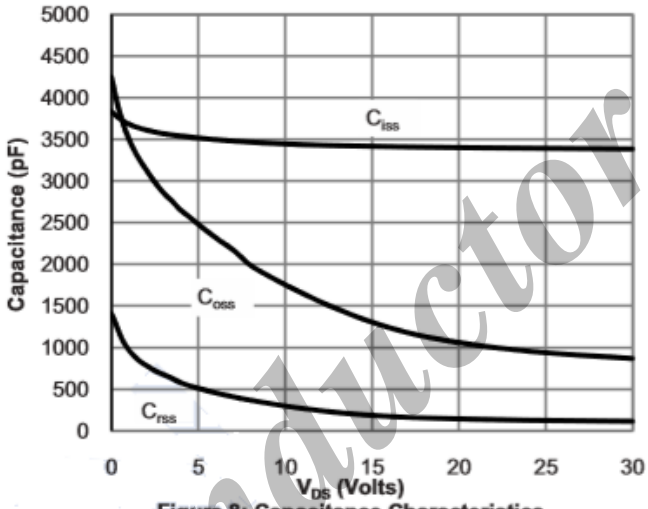


Figure 8: Capacitance Characteristics

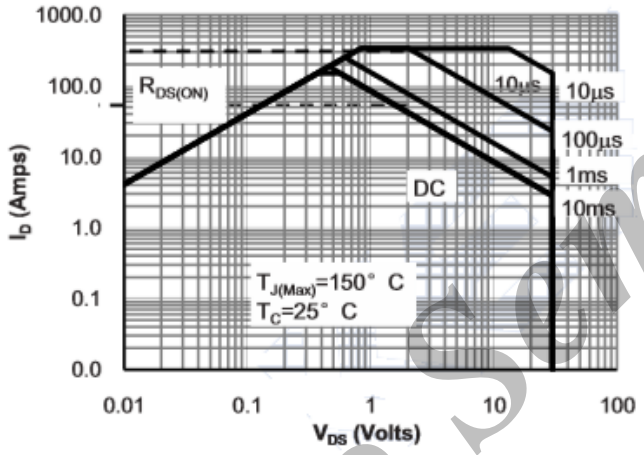


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

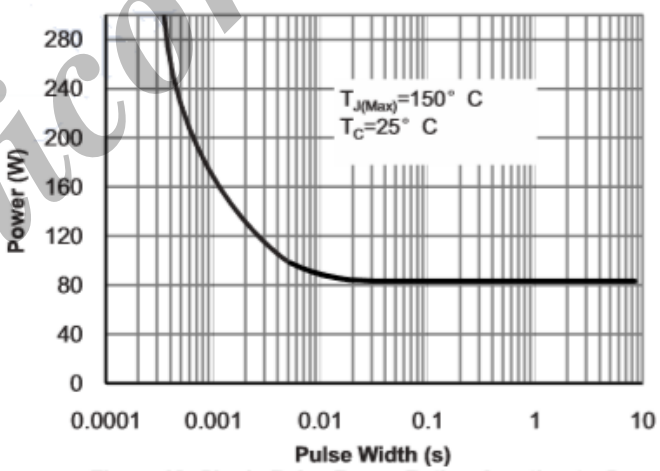


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

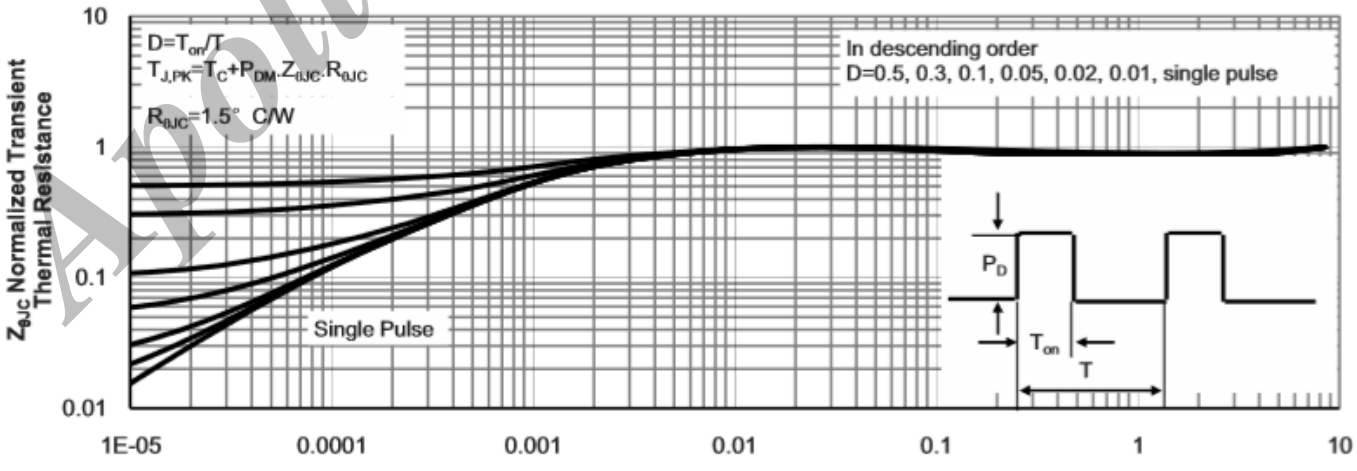


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

- **Typical Characteristics**

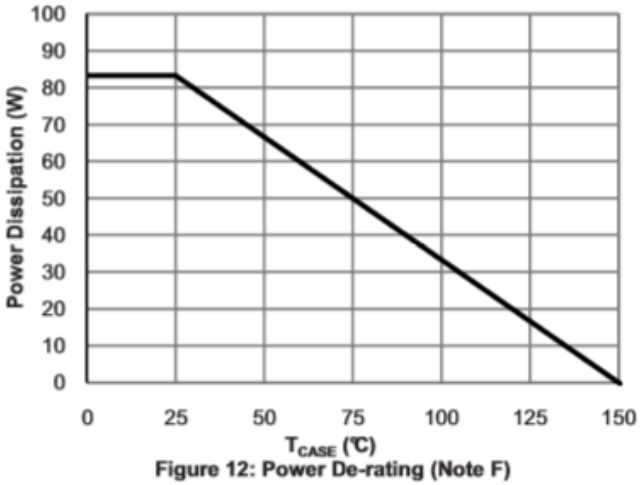


Figure 12: Power De-rating (Note F)

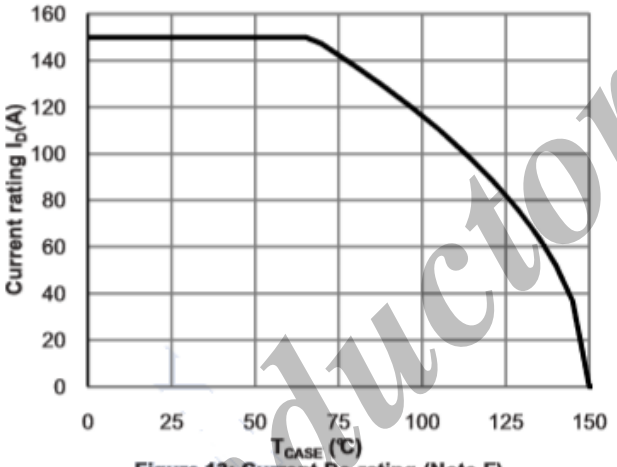


Figure 13: Current De-rating (Note F)

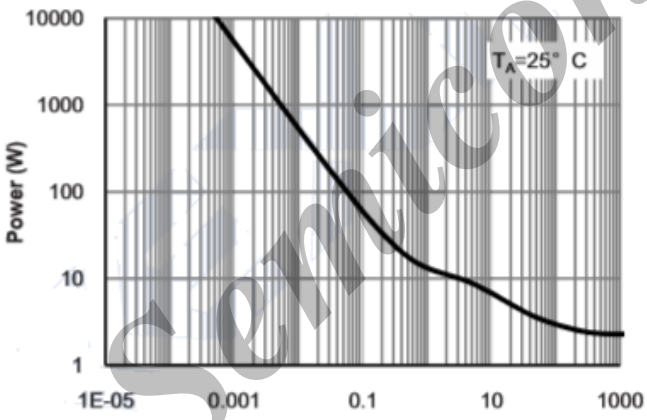


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

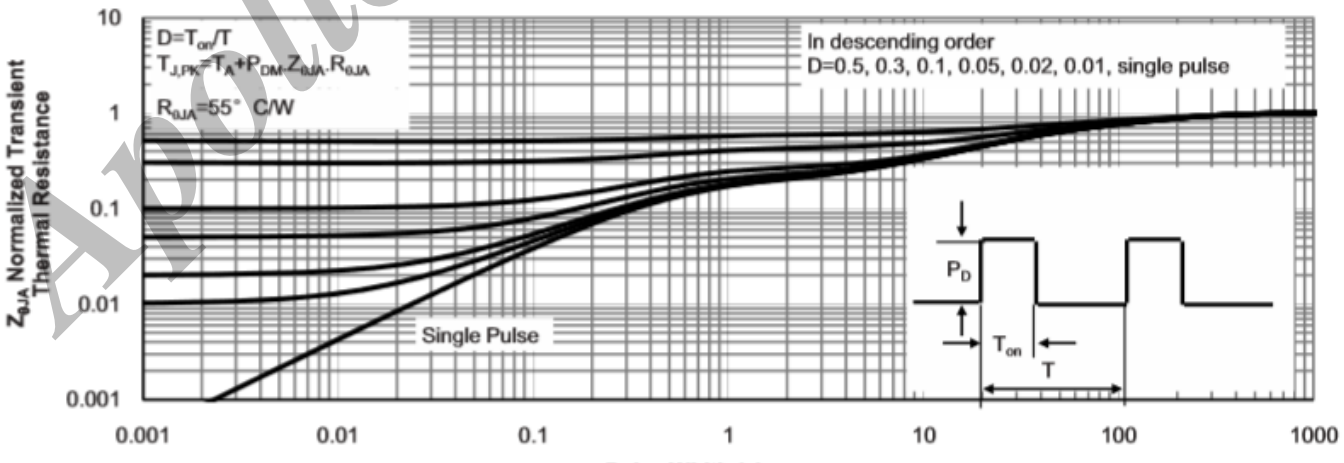
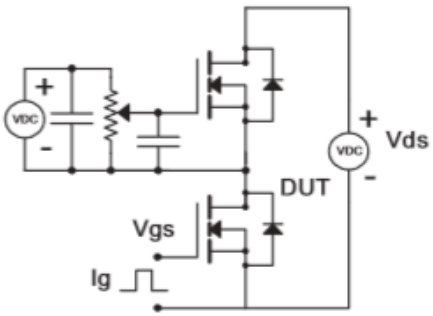
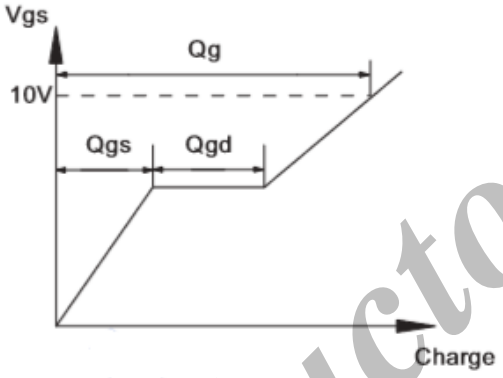


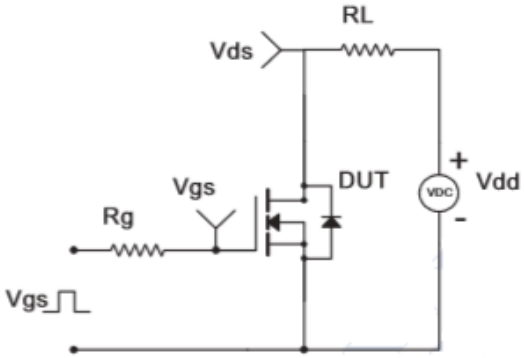
Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

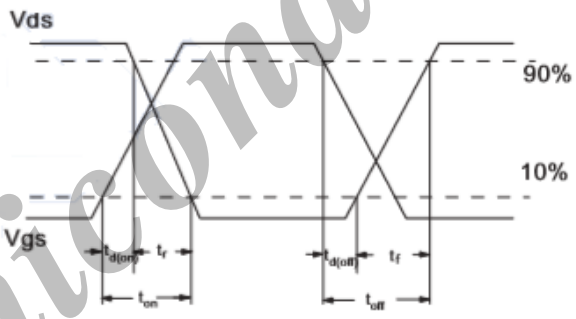
Gate Charge Test Circuit & Waveform



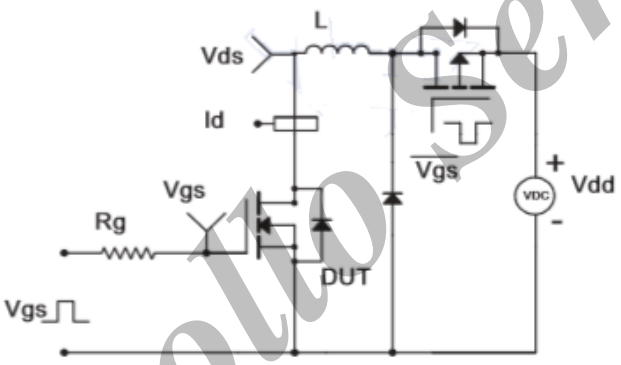


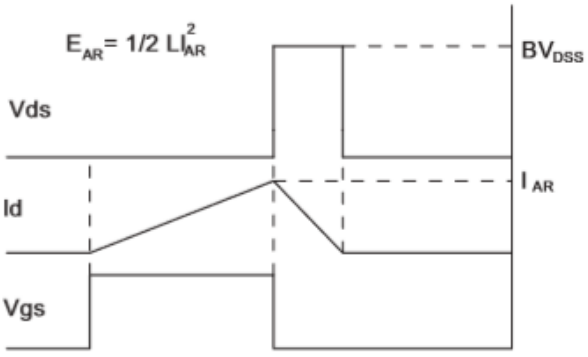
Resistive Switching Test Circuit & Waveforms



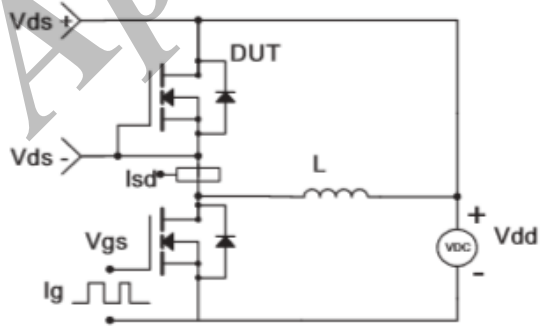


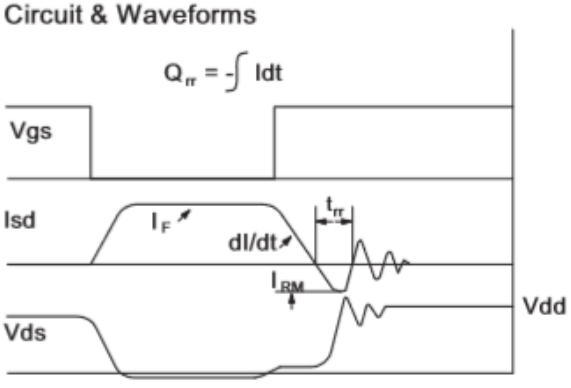
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



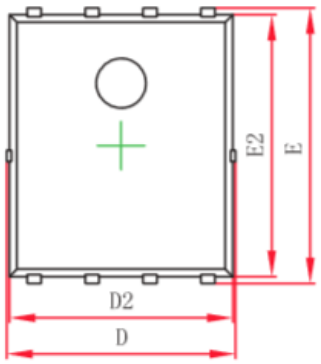


Diode Recovery Test Circuit & Waveforms

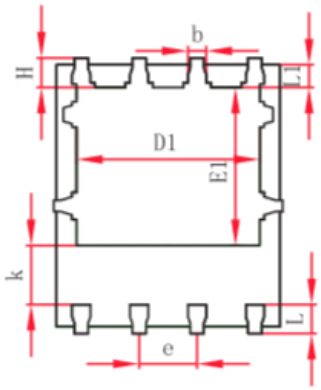




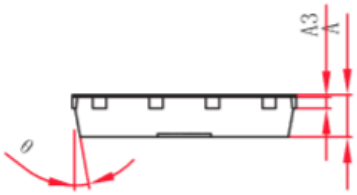
- **DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions**



Top View



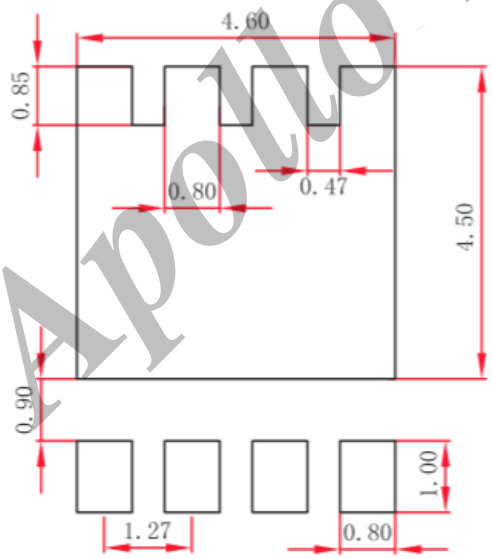
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.994	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

■ DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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